Dual-Gated Topological Insulator Thin-Film Device for Efficient Fermi-Level Tuning

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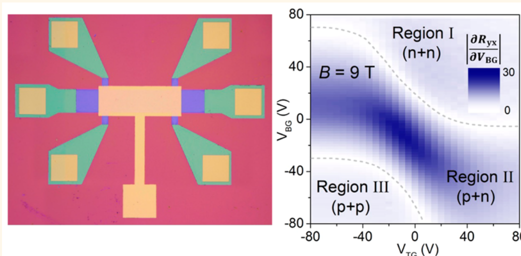
ABSTRACT Observations of novel quantum phenomena expected for three-dimensional topological insulators (TIs) often require fabrications of thin-film devices and tuning of the Fermi level across the Dirac point. Since thin films have both top and bottom surfaces, an effective control of the surface chemical potential requires dual gating. However, a reliable dual-gating technique for TI thin films has not yet been developed. Here we report a comprehensive method to fabricate a dual-gated TI device and demonstrate tuning of the chemical potential of both surfaces across the Dirac points. The most important part of our method is the recipe for safely detaching high-quality, bulk-insulating $(Bi_{1-x}Sb_x)_2Te_3$ thin films from sapphire substrates and transferring them to Si/SiO_2 wafers that allow back gating. Fabrication of an efficient top gate by low-temperature deposition of a SiN_x dielectric complements the procedure. Our dual-gated devices are shown to be effective in tuning the chemical potential in a wide range encompassing the Dirac points on both surfaces.



KEYWORDS: topological insulator · $(Bi_{1-x}Sb_x)_2Te_3$ · electrostatic gating · MBE · Dirac fermion

Three-dimensional (3D) topological insulators (TIs) harbor spin-momentum-locked surface states forming a Dirac cone.[1−3] The resulting spin-nondegenerate Dirac fermions inhabiting the surface of 3D TIs hold promise for various novel phenomena such as topological magnetoelectric effects,[4,5] proximity-induced topological superconductivity associated with Majorana fermions,[6] and topological exciton condensation,[7] all of which would provide fundamentally new device principles. Realizations of those novel phenomena require fine control of the surface chemical potential, which is best achieved by electrostatic gating.

So far, both back gating[8,9] and top gating[10−13] have been successfully applied to 3D TI thin films, but with a single gate the chemical potential of only one surface (bottom or top) can be effectively tuned, and the other surface is not controlled simultaneously unless the samples are ultrathin.[14] Unfortunately, this is not sufficient for many applications: For example, the topological magnetoelectric effects require the chemical potential of the whole surface of a 3D TI to be tuned to the Dirac point, which is to be gapped by time-reversal-breaking perturbations; also, the topological exciton condensation requires the top and bottom surfaces to contain equal numbers of Dirac electrons and holes, respectively (or *vice versa*). Furthermore, in a new type of topological insulator called a topological crystalline insulator,[3] dual gating will controllably break mirror symmetry and allow a fundamentally new type of transistor device.[15] Obviously, efficient dual-gating techniques should be developed for future studies of 3D TIs.

In this paper, we report our successful development of a comprehensive method to fabricate a highly tunable dual-gated TI device based on bulk-insulating $(Bi_{1-x}Sb_x)_2Te_3$ thin films. Our device is made of large-area thin films rather than exfoliated single crystals, and all fabrication processes are done only with photolithography, both of which are important ingredients for future industrial applications. In the case of nanodevices based on exfoliated platelets, back gating is relatively easy, because one can directly exfoliate the TI materials onto Si/SiO_2 substrates that allow

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back gating. The back gating is more difficult for thin-film devices, because epitaxial growth of TI thin films on a thin dielectric is not a straightforward task. In the past, a $SrTiO_3$ substrate has been used for back gating, utilizing its ultrahigh dielectric constant at low temperatures, but this limits both the choice of better substrates for film growth and the working temperature of the back gate. In terms of the film quality, a sapphire substrate is among the best for Bi_2Se_3[16,17] and Bi_2Te_3,[18] but gating through a sapphire substrate is impractical. Recently, it was reported[19] that high-quality Bi_2Se_3 films grown on a sapphire substrate can be transferred to other substrates by using buffered oxide etch (BOE) or a potassium hydroxide (KOH) solution to peel off the films from the sapphire substrates. The present work builds on this progress. Our device is based on thin films of bulk-insulating $(Bi_{1-x}Sb_x)_2Te_3$[20] grown on sapphire substrates by molecular beam epitaxy (MBE), which are subsequently peeled off and transferred to a Si/SiO_2 substrates. Since we found that neither BOE nor KOH works well for $(Bi_{1-x}Sb_x)_2Te_3$, we have developed an improved, damage-free method for the film transfer.

Fabrications of top gates on TIs are notorious for damaging the top surface mobility and introducing localized states to pin the chemical potential, which works against effective gate tuning;[21] nevertheless, several groups have recently made progress in this respect. For example, our group employed hot-wire chemical vapor deposition (CVD) of a SiN_x dielectric layer at low temperature and successfully fabricated an efficient top gate without degrading the mobility.[11] Other groups employed atomic-layer deposition (ALD) of an Al_2O_3 dielectric layer at low temperature[12] or used exfoliated h-BN platelets[22] for preserving the quality of the surface beneath the top gate. In the present work, we used the SiN_x dielectric layer deposited by hot-wire CVD to fabricate a top gate. The dual-gate structure of our device turns out to be effective in tuning the chemical potential of the top and bottom surfaces across the Dirac point.

RESULTS AND DISCUSSION

The epitaxial $(Bi_{1-x}Sb_x)_2Te_3$ (hereafter called BST) thin films were grown on sapphire (0001) substrates by using an MBE technique (see the Methods for details).[23] In this paper, we focus on 17 nm thick films with $x = 0.15$, which is optimized for the bulk-insulating property. The thickness was measured with an atomic-force microscope (AFM), which is also used for confirming the epitaxial growth with large, atomically flat terraces (Figure 1A). The X-ray diffraction data for small angles show clear Kiessig fringes (Figure 1B), which testifies to the homogeneity of the thickness.

After the MBE growth, we transferred the BST films from sapphire to Si/SiO_2 substrates. According to the previously reported method, which works for Bi_2Se_3 films,[19] in order to peel off the film from the sapphire substrate, the film needs to be floated on BOE or KOH solution. However, in the case of the BST films, we found that both BOE and KOH cause problems. The BST films cannot be detached in BOE; in KOH, the peeling-off occurs smoothly, but the BST film is chemically attacked and degraded (see the Supporting Information). Therefore, we developed a new transfer method using distilled water to avoid the degradation of the BST film due to KOH. As demonstrated in the Supporting Information, the morphology of the films does not present any noticeable degradation after the transfer (Figure S2); also, the carrier concentration and the mobility of the BST films transferred by this method are comparable to those of the as-grown films (Figure S3).

The transfer of the films was done in the steps described in detail in the Methods section (see Figure 2

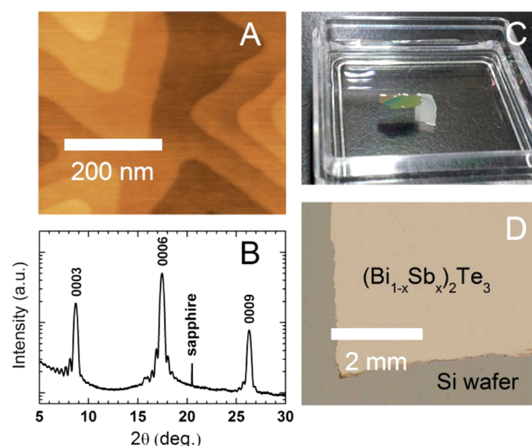

Figure 1. (A) AFM image of a 17 nm thick $(Bi_{1-x}Sb_x)_2Te_3$ film. (B) Low-angle X-ray diffraction patterns of a 28 nm thick $(Bi_{1-x}Sb_x)_2Te_3$ film. (C) After the peeling-off, the detached $(Bi_{1-x}Sb_x)_2Te_3$/PMMA bilayer floats on pure water, while the sapphire substrate sinks down. (D) Optical image of a $(Bi_{1-x}Sb_x)_2Te_3$ film transferred onto a silicon wafer.

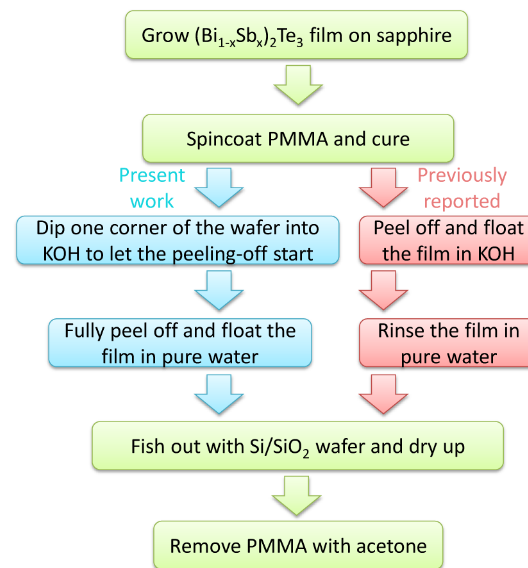

Figure 2. Diagram of the film-transfer process.

for a diagram). Essentially, the film is spin-coated with the polymethyl methacrylate (PMMA), and the peeling-off process of the BST/PMMA bilayer is initiated by dipping only one corner of the substrate into a KOH aqueous solution, followed by complete detachment in distilled water (Figure 1C). The BST/PMMA bilayer floating on the water is taken out with a Si or Si/SiO_2 wafer, and the PMMA layer is removed with acetone to complete the transfer process (Figure 1D). After the transfer of the film to the Si/SiO_2 wafer, we fabricated the top gate using the process described in ref 11 (see Methods section for details). The optical photograph and the schematic of our device are shown in Figure 3.

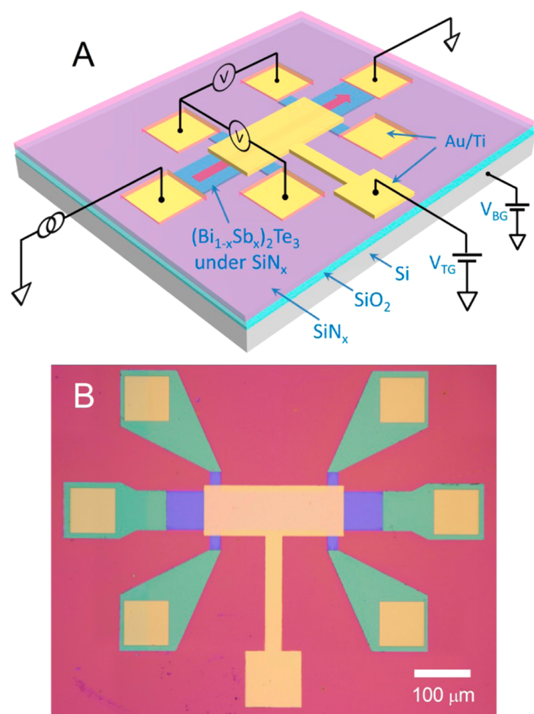

Figure 3. (A) Schematics of the device structure and measurement configuration. (B) Optical image of a typical device.

The measurements of the sheet resistance (R_{sh}) and the Hall resistance (R_{yx}) were made on the Hall bar at T = 1.8−300 K. The top- and back-gate voltages (V_{TG} and V_{BG}, respectively) were applied in the range of ±90 V. We note that, when the top-gate voltage is cycled, a hysteresis due to trapped charges was observed in both R_{sh} and R_{yx}; hence, to avoid confusion, all the presented curves were taken with a decreasing gate voltage from +90 to −90 V.

Figure 4 shows a comparison of the gating effects seen in R_{sh} and R_{yx} (in B = 9 T) at T = 1.8 K for three gating configurations: top, back, and dual gating. In the case of dual gating, the same voltage was applied to both top and back gates.

In order to understand the gating result, one should notice the existence of a finite capacitive coupling between the top and bottom surface states for thin bulk-insulating TI devices (see Supporting Information for full modeling).[11,22] Due to the capacitive coupling, the two surfaces are not tuned independently. When a voltage is applied to a single gate, the chemical potential of the other surface is also affected. Our previous results[11] show that the coupling ratio (defined as $\Delta N_{bot}/\Delta N_{top}$, when ΔV_{TG} is applied) is about 50% around the Dirac point for a 20 nm thick BST film. In the present work, the thickness of the film is 17 nm, suggesting that the coupling can be even stronger.

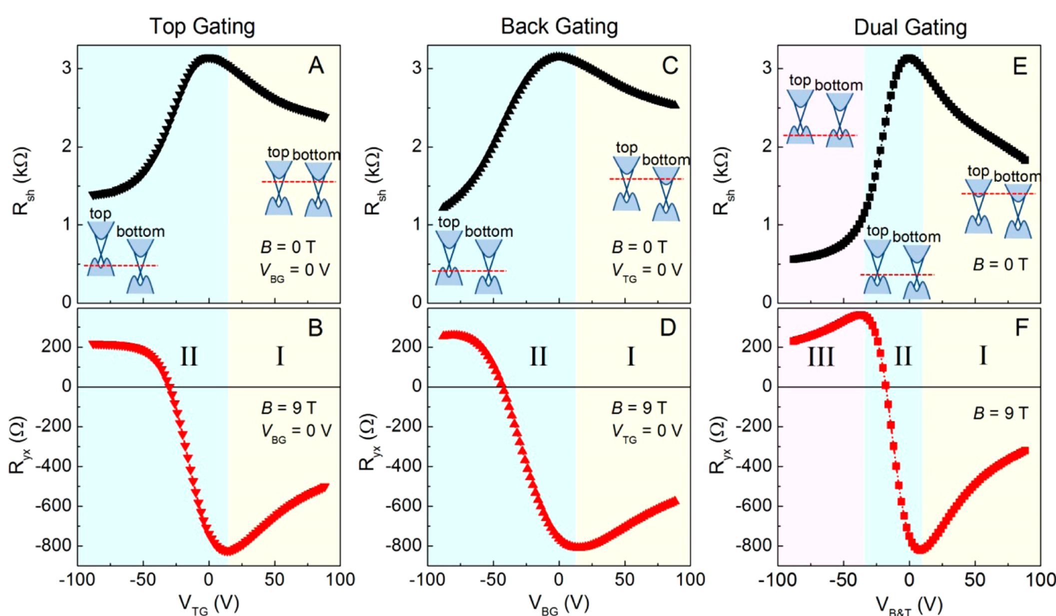

Figure 4. Gate-voltage dependences of sheet resistance (R_{sh}) and Hall resistivity (R_{yx}) for three different gating configurations: (A, B) top gating, (C, D) back gating, and (E, F) dual gating.

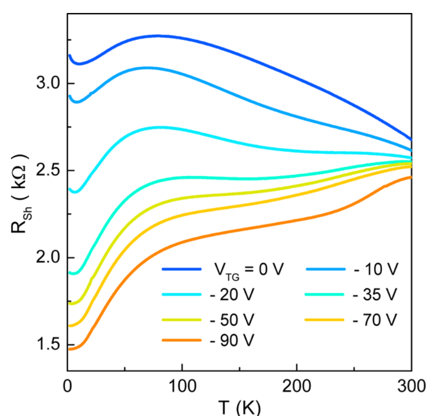

Figure 5. Temperature dependences of the sheet resistance (R_{sh}) at different top-gate voltages.

In the 17 nm thick BST film used for the dual-gated device, at zero gate voltage, it turned out that the carrier type and carrier concentrations of the two surfaces are different, possibly due to the difference in band bending caused by different interfaces: The top surface accommodates a low concentration of p-type carriers, and thus its Fermi level is slightly below the Dirac point; on the other hand, the bottom surface is n-type with a relatively high carrier concentration, corresponding to a Fermi-level position well above the Dirac point.

Due to the high initial concentration of n-type carriers on the bottom surface, for the single top gating (Figure 4A,B) or back gating (Figure 4C,D), only the Fermi level of the top surface can be tuned across the Dirac point, corresponding to the single negative peak in $R_{yx}(V)$ (Figure 4B,D) and the peak in R_{sh} at a similar gate voltage (Figure 4A,C). For the convenience of further discussions, we divide the single-gating data (Figure 4A–D) into two regions according to the difference in band diagrams. In region I, R_{yx} is negative, and $|R_{yx}|$ increases upon scanning the gate voltage in the negative direction; This means that both surfaces are n-type. On the boundary with region II, the top surface goes across the Dirac point and becomes p-type, and therefore $|R_{yx}|$ starts to decrease before it reaches zero and changes sign. The sign change indicates that the sample becomes p-type dominated. However, the absence of a positive peak in $R_{yx}(V)$ suggests that the bottom surface is still n-type.

In contrast, in the case of dual gating (Figure 4E,F), the gate-voltage dependence of R_{yx} presents *both* negative and positive peaks, and a new region (region III) shows up. In region III, R_{yx} is positive, and $|R_{yx}|$ decreases upon scanning the dual-gate voltage ($V_{B\&T}$) in the negative direction; this means that both surfaces are now tuned to be p-type. Therefore, with the help of additional positive carriers provided by the top gate, the back gate is now able to bring down the chemical potential of the bottom surface to cross the

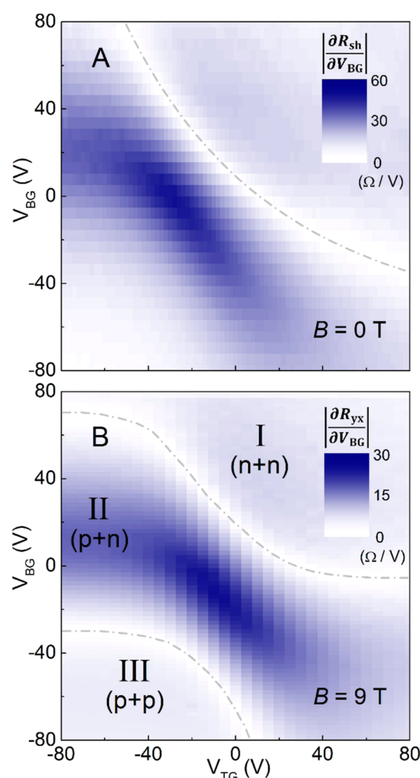

Figure 6. 2D plots of (A) $|\partial R_{sh}/\partial V_{BG}|$ and (B) $|\partial R_{yx}/\partial V_{BG}|$ as a function of top-gate and back-gate voltages. These data were taken on a different device on the same wafer based on the same batch of the BST film. The dash-dotted lines are a guide to the eyes to trace the locations of the "white bands", which correspond to the locations of the peaks (*i.e.*, zero slope) in the raw data.

Dirac point. It is useful to note that in our device the change in R_{sh} upon dual gating is as large as a factor of 6 (Figure 4E), which is among the largest ever reported for TI thin-film devices except for the cases of quantum Hall[13,24] or quantum anomalous Hall[12,25,26] effects. The temperature dependences of R_{sh} for various V_{TG} from 0 to −90 V are shown in Figure 5. It demonstrates that the gate works effectively in modifying the resistance of the device even at room temperature, which overcomes the working temperature limit of the back gate based on $SrTiO_3$.

We have also done experiments to scan both V_{TG} and V_{BG} independently (the measurements were made on a different device). Figure 6 shows false-color mappings of $|\partial R_{sh}/\partial V_{BG}|$ and $|\partial R_{yx}/\partial V_{BG}|$ in the V_{BG} *vs* V_{TG} plane. The white color corresponds to a positive or negative peak (*i.e.*, zero slope), and hence the two white bands in the $|\partial R_{yx}/\partial V_{BG}|$ map (Figure 6B) roughly show where the Dirac point is accessed; in other words, the two white bands in Figure 6B separate the regions I, II, and III indicated in Figure 4. By comparing the locations of the white bands in Figure 6A and B, one can see that the peak in R_{sh} does not necessarily mean that the chemical potential is at the Dirac point in a dual-gate device.[22] The raw data before taking the

derivative are available in Figure S3 of the Supporting Information.

CONCLUSION

We have presented a comprehensive method to realize highly efficient dual gating of TI thin films. It combines the transfer of high-quality epitaxial thin films grown on sapphire onto a Si/SiO_2 wafer and top-gate fabrication by using a low-temperature deposition of SiN_x with hot-wire CVD. This method is based on large-area thin films and employs only photolithography, both of which are favorable for future industrial applications. We demonstrate that the dual gating allows tuning of the chemical potentials of the top and bottom surfaces across the Dirac point, which is manifested in the $V_{B\&T}$ dependence of R_{yx} showing a sharp sign change bound by two peaks, and also in R_{sh}, changing by 6 times with $V_{B\&T}$. This dual-gating method opens exciting opportunities to realize various novel phenomena expected for 3D TIs.

METHODS

MEB Growth of BST Films. The 17 nm thick BST films were grown on sapphire (0001) substrates by MBE. The co-deposition of Bi and Sb (with a flux ratio of 1:5.5) was done in three steps at different substrate temperatures: 5 min at 230 °C, 5 min at 280 °C, and 21 min at 325 °C. The morphology and thickness of the films were measured with AFM.

Transfer of BST Films. After the growth, the BST film was spin-coated with PMMA at 5000 rpm for 1 min and cured at 170 °C for 3 min. Then one corner of the substrate was dipped into a 5% KOH aqueous solution to initiate the detachment. During this initial stage, only a small portion of the film at the corner was exposed to the KOH solution. After several minutes, the BST/PMMA bilayer started to separate from sapphire at the corner. At that point, the substrate was taken out from the KOH solution and the separated corner was then dipped into distilled water; due to the strong surface tension of water, the detached part of the BST/PMMA bilayer would float on the water surface. Then the whole substrate was slowly inserted into the water; during this process, the BST/PMMA bilayer feels a buoyancy force to make it detach from the substrate due to the surface tension of the water. Eventually, the whole BST/PMMA bilayer was fully detached and floated on the water surface (Figure 1C). After that, the floating BST/PMMA bilayer was taken out with a Si/SiO_2 wafer (SiO_2 thickness of 150 nm), dried at room temperature, and treated with acetone to remove PMMA. Finally, the transferred BST film (Figure 1D) was annealed at 120 °C under vacuum for 2 to 7 h to fully get rid of residual water; we found that this final annealing process promoted the insulating property of the film.

Device Fabrication. The BST film was patterned into a Hall-bar shape with photolithography and wet etching. The etchant is 1 HCl/0.8 H_2O_2/8 CH_3COOH/16 H_2O (volume ratio); the mass concentrations of the first three solutions are 36%, 33%, and 99.7%, respectively. Next, metal contacts (5 nm Ti and 50 nm Au) were fabricated with photolithography, thermal evaporation, and lift-off. Then a 200 nm SiN_x dielectric layer was deposited with hot-wire CVD at $T < 80$ °C, covering the whole wafer. After that, the SiN_x layer above the metal contacts was removed by photolithography and reactive-ion etching (CF_4/Ar flow: 20/5 sccm, pressure: 3 Pa, power: 100 W, duration: 3 min). Finally, a top-gate electrode was fabricated by photolithography and Ti/Au deposition.

Transport Measurements. The measurements were performed using a standard ac lock-in technique in a cryostat with a base temperature of 1.8 K in magnetic fields up to 9 T. The excitation current was 1 μA. The gate voltages were applied using Keithley 2400 source meters.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Comparison of the morphology of BST films before and after treatment with a 5% KOH solution, morphology of the BST film after transfer, comparison of transport properties of BST films before and after transfer, magnetic-field dependences of the Hall resistivity at various $V_{B\&T}$, V_{BG} dependences of R_{sh} and R_{yx} at various V_{TG}, and an effective model of the dual gating. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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